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Paper:

A Highly Efficient and Reliable Power Scheme Using Improved Push-Pull Forward Converter for Heavy-Duty Train Applications

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Electronically controlled pneumatic (ECP) brake systems have become popular in heavy-duty train applications because of their advantages, which include shorter stopping distances, improved handling, and less brake-shoe and wheel wear. In ECP brake systems, an improved power supply is required to support efficient and reliable operations. In this paper, we propose a new power converter for ECP brake systems, which is derived from a conventional push-pull converter. As opposed to conventional push-pull converters, we insert a clamping capacitor into the proposed circuit. This clamping capacitor simultaneously enables a greater number of operation modes for the proposed converter and absorbs the voltage spikes in the switch. The proposed converter is more suited for ECP brake applications that require high power, low voltage ripple, and high impedance. We theoretically analyze the proposed converter, and present the design guidelines. Further, we discuss the modeling and control aspects. We demonstrate the operations of the proposed model by performing both simulations and experiments.

Keywords: push-pull forward, output impedance, high efficiency, ECP

1. Introduction

Recently, there has been an increased utilization of heavy-duty trains that travel at high speed and high capacity. However, the increased operation speed and capacity has introduced new challenges for the design of conventional pneumatic brake systems. These challenges include limitations on a trains length and operation speed, and derailment issues need to be considered [1, 2]. In order to address these challenges, the conventional pneumatic brake system has been replaced with electronically controlled pneumatic (ECP) brake systems in heavy-duty trains. ECP brake systems have advantages including a shorter stopping distance, higher energy efficiency, and less wear of the wheel and brake shoe [3, 4].

Heavy-duty trains have more than 200 cars with lengths exceeding 3000 m [4]. It is challenging to power an ECP brake system that is distributed over 200 cars. In an ECP brake system, the power and signal are transmitted through a shared conductor. To ensure safe and reliable operation, the power level should be up to 2.5 kW, and the conductor should have high efficiency. In addition, the ripple and harmonic of the output voltage need to be suppressed. To meet these requirements, the converter topology and output impedance should be considered. Moreover, a robust controller is essential to ensure steady-state and dynamic performance.

Of the high-efficiency DC-DC converters, buck-boost converters [5, 6] are more widely used for low-power applications, but they cannot provide the galvanic isolation that is required for some applications because of safety concerns. For isolated topologies, forward converters [7, 8] and flyback converters [9] require an additional magnetizing reset circuit. The low utilization of isolation transformers limit the power density and efficiency of these topologies. Push-pull converters [10] are suitable for high-power applications. However, a high voltage stress, which is up to twice the input voltage, is applied to the primary-side power switches. In addition, the transformer leakage inductance energy cannot be absorbed very well, resulting in lower efficiency. The push-pull forward (PPF) converter [11, 12] is a good candidate for ECP brake applications because of its ability to achieve high efficiency at high power levels, while simultaneously achieving galvanic isolation. Further, the clamping capacitor in PPF converters can help to improve the power-conversion efficiency [13]. However, the voltage fluctuation across the rectifier diode remains a challenge in the PPF topology. One method is to dampen the oscillations using passive snubbers [14, 15]. Nevertheless, the use of snubber circuits limits the available duty cycle [16], and these snubber circuits can become overheated under transient load conditions.

As discussed above, ECP power supply systems require high power, high impedance, low noise, and low ripple. In order to meet these requirements in ECP brake applications, in this paper, we propose a new DC-DC converter with a lossless snubber circuit. We employ an improved PPF circuit on the primary side of the isolation transformer to enable high-power applications. We present a modified non-dissipative snubber circuit that reduces the voltage stress of the rectifier diodes and improves the

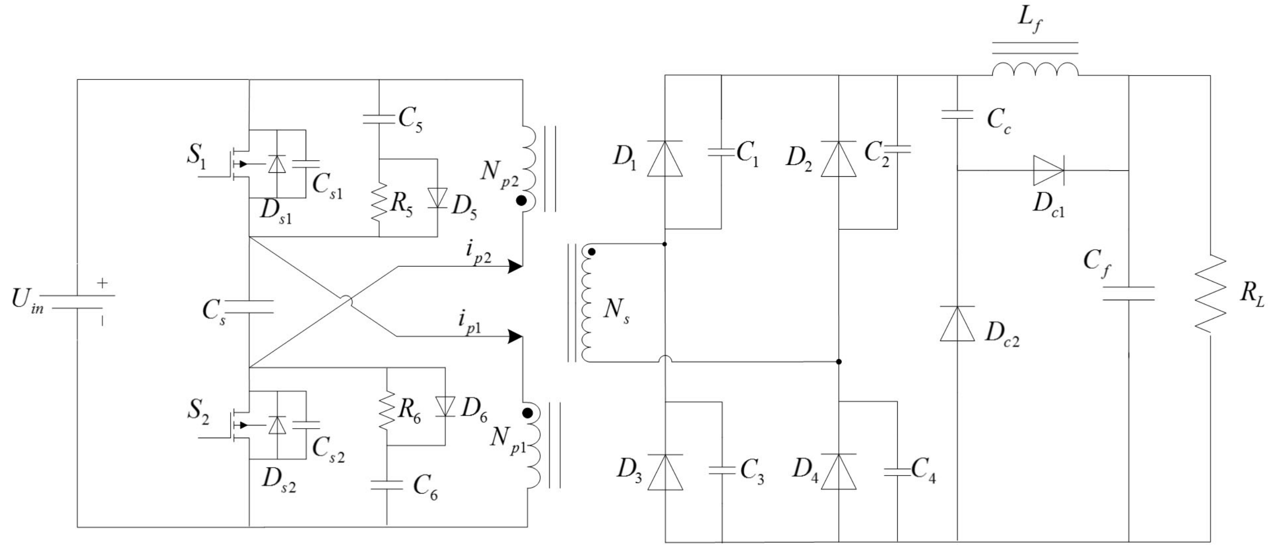

Fig. 1. Schematic of the proposed converter.

power-conversion efficiency. In the design of the DC-DC converter, the control loop needs to be well compensated in order to ensure good steady-state and dynamic performance of the converter. We designed a type-II compensation network to provide high bandwidth and phase margin to the converter. We carefully designed the output impedance of the proposed converter in order to limit the interference of the power supply on the communication system. Finally, we built a 2.5 kW converter prototype in the lab to demonstrate the operations and show the advantages of the proposed converter.

The contributions of this paper are twofold. First, we designed a high-efficiency DC-DC converter. By using an improved PPF topology and lossless snubber circuit, it achieved high efficiency at high power levels. Second, we carefully designed the feedback-loop compensation network and the output impedance of the proposed converter in order to obtain good dynamic and steady-state performance and limit the interference on the communication system.

The rest of this paper is organized as follows. In Section 2, we first analyze the operating principles and design considerations of the proposed circuit. Then, we discussed the modeling of the proposed converter and the design of the compensation network in Section 3. After that, we present the simulations that were conducted, and we present the results in Section 4. We performed experiments using a lab-built prototype, and the corresponding results are presented in Section 5. Finally, we summarize the study and conclude the paper in Section 6.

2. System Circuit and Operation Principle

2.1. Topology Description

The proposed converter topology is shown in **Fig. 1**. S_1 and S_2 are the main power switches. D_{s1} and D_{s2} are the anti-parallel diodes of the power switches, while C_{s1} and C_{s2} are the output capacitances. A transformer with two primary windings and one secondary wingding is used to provide galvanic isolation. C_s is the clamping capacitor and the RCD circuit ($R_5C_5D_5, R_6C_6D_6$) is used to absorb the energy stored in the transformer leakage inductances. The secondary side of the transformer is a full-bridge rectifier composed of diodes D_1 to D_4, which are in parallel with external capacitors C_1 to C_4. C_c, D_{C_1}, and D_{C_2} constitute a CDD (one capacitor and two diodes) non-dissipative snubber. The output inductor L_f and capacitor C_f form a low-pass filter.

2.2. Operation Principles

The following assumptions were made for the simplification of the analysis.

1) All the switches and diodes are ideal.

2) The voltage of the clamping capacitor C_s in steady state is constant, and is equal to the input voltage.

3) The output inductor is large enough. In the steady state, the average value of the output current is $I_o = V_{out}/R_o$.

4) The turns ratio of the transformer is $N = N_s/N_p$, where $N_{p1} = N_{p2} = N_p$.

5) The magnetizing inductances L_{m1} and L_{m2} and the leakage inductances on the primary side of the transformer L_{k1} and L_{k2} can be considered as being equal, $L_{m1} = L_{m2} = L_m$ and $L_{k1} = L_{k2} = L_k$. L_σ represents the leakage inductances of the transformer in secondary side.

6) D is the duty ratio of S_1 and S_2, $D = T_{on}/T_s$, T_{on} is the switching on time of a cycle, and T_s is the switching cycle.

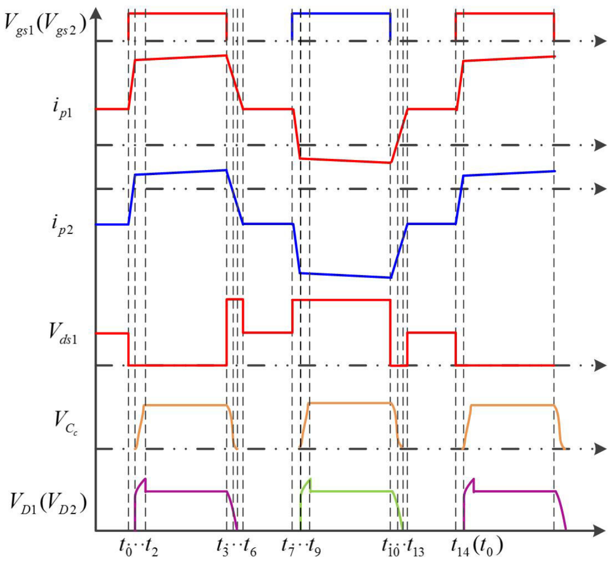

Fig. 2. Theoretical waveforms obtained during steady-state operation of the proposed converter.

Figure 2 shows the theoretical waveforms obtained during the steady-state operation of the proposed converter, V_{gs1} and V_{gs2} are the corresponding driving signals of S_1 and S_2, and i_{p1} and i_{p2} are the primary-side winding currents that are shown in **Fig. 1**. V_{ds1} is the drain-source voltage of the main power switch S_1, V_{D1} and V_{D2} are the voltages of the rectifier diodes, and V_{C_c} is the voltage of C_c in the lossless snubber circuit. The operation of the proposed converter is divided into 12 operation modes (t_0 – t_{14}).

1) Mode 1 [$t_0 - t_1$]: Before t_0, the switches are off. The primary windings of the transformer are in series with the clamping capacitor, and the energy stored in the leakage inductances of the transformer is delivered to the clamping capacitor. The current is called a circulating current I_a. At time t_0, the switch S_1 is turned on, as shown in **Fig. 3(a)**. The input voltage and clamping capacitor voltage are added to the leakage inductances of N_{p1} and N_{p2}. The current i_{p1} increases rapidly. The current through N_{p2} passes from negative to positive. The current of the primary-side windings can be represented as

$$\begin{cases} i_{p1}(t) = I_a + \dfrac{U_{in}}{L_k}(t-t_0) \\ i_{p2}(t) = -I_a + \dfrac{U_c}{L_k}(t-t_0) \end{cases} ; \ t \in [t_0, t_1]. \quad . \quad . \quad (1)$$

The current through the filtering inductor at time t_1 is $I_{L\min}$, and the duration of this mode is

$$\Delta t_{0-1} = \frac{N I_{L\min} L_k}{2U_{in}}. \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (2)$$

2) Mode 2 [$t_1 - t_2$]: Before t_1, the CDD circuit does not work, and the inverse voltage of diode D_{c1} is V_o. As shown in **Fig. 3(b)**, when i_{D2} reaches the negative maximum, the snubber circuit begins to work, and the instant inverse voltage of capacitors C_1 and C_2 is V_o. C_c is charged through $C_c - D_{c1} - C_f$. The voltage across capacitor C_c is denoted as

$$V_{C_c} = N \cdot U_{in} - V_o[1-\cos(w(t-t_1))] \ ; \ t \in [t_1, t_2], \quad (3)$$

where w is the resonant frequency of the secondary-side leakage inductance and capacitor C_c, and $w = 1/\sqrt{L_\sigma \cdot C_c}$. The voltage across the buffering capacitor increases from zero, and it reaches the maximum $V_{C_c} = 2(N \cdot U_{in} - V_o)$ at time t_2. Because the diode D_{c1} switches on, the maximum inverse voltage across diodes D_2 and D_3 is

$$V_{D_2} = V_{D_3} = \max(V_{C_c}) + V_o = 2NV_{in} - V_o. \quad . \quad . \quad (4)$$

3) Mode 3 [$t_2 - t_3$]: As shown in **Fig. 3(c)**, the energy starts to be transferred to the secondary side from t_1, and the process continues until t_3. During this period, the input voltage and the clamping capacitor voltage are added to the two secondary-side inductors, leakage inductor, and the equivalent inductor N^2L_f. On the secondary side of the transformer, the voltages across diodes D_2, D_3 decrease to NV_{in}, and diode D_{c1} is turned off because of the reverse voltage. The entire load current is passed through D_1 and D_4. The currents through the primary-side windings are as shown in Eq. (5).

$$\begin{cases} i_{p1}(t) = I_a + \dfrac{NI_{L\min}}{2} \\ \qquad + \left(\dfrac{U_{in}}{2L_m} + \dfrac{N^2 U_{in}}{2L_f}\right)(t-t_1) \ ; \ t \in [t_1, t_3] \\ i_{p2}(t) = -I_a + \dfrac{NI_{L\min}}{2} \\ \qquad + \left(\dfrac{U_c}{2L_m} + \dfrac{N^2 U_c}{2L_f}\right)(t-t_1) \ ; \ t \in [t_1, t_3] \end{cases}$$

$$. \quad (5)$$

At time t_3, switch S_1 is turned off. The duration of mode 2 and mode 3 is

$$\Delta t_{1-3} = DT_s - \Delta t_{0-1}. \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (6)$$

4) Mode 4 [$t_3 - t_5$]: As shown in **Fig. 3(d)**, S_1 is turned off at time t_3. The body diode of S_2 conducts current, which makes the voltage across S_1 clamp to two times the value of the input voltage. The energy stored in the leakage inductor of winding N_{p1} is released to the clamping capacitor through S_2, while the energy stored in the leakage inductor of winding N_{p2} is released to the input source. The winding currents can be calculated as

$$\begin{cases} i_{p1}(t) = i_{p1}(t_3) - \dfrac{U_c}{L_k}(t-t_3) \\ i_{p2}(t) = i_{p2}(t_3) - \dfrac{U_{in}}{L_k}(t-t_3) \end{cases} ; \ t \in [t_3, t_5]. \quad . \quad . \quad (7)$$

On the secondary side of the transformer, the currents through D_1 and D_4 begin to decrease. The energy in the buffer capacitor C_c is released through $C_c \rightarrow L_f \rightarrow C_f \rightarrow D_{c2}$. The relationship is

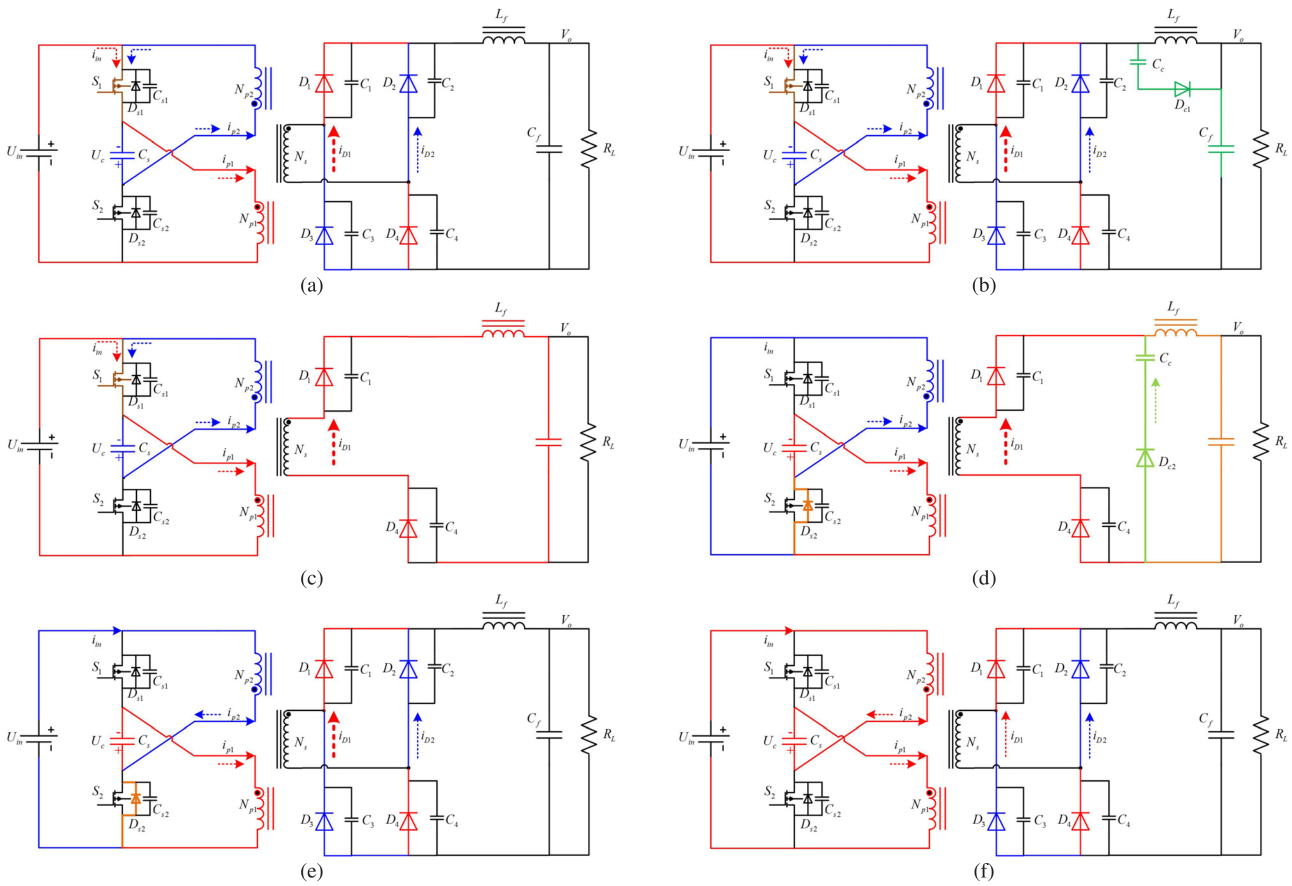

Fig. 3. Operation modes of the converter. (a) Mode 1: $t_0 < t < t_1$, (b) Mode 2: $t_1 < t < t_2$, (c) Mode 3: $t_2 < t < t_3$, (d) Mode 4: $t_3 < t < t_5$, (e) Mode 5: $t_5 < t < t_6$, and (f) Mode 6: $t_6 < t < t_7$.

$$\begin{cases} V_{C_c} = N \cdot U_{in} - N \cdot U_{in} \\ \qquad - V_o[1 - \cos(w(t - t_3))] \qquad ; \; t \in [t_3, t_4] \\ V_{C_c} = N \cdot U_{in} + N \cdot U_{in} - \dfrac{I_o}{C_c}(t - t_4) \\ \qquad - V_o\sqrt{1 - \left[\dfrac{I_o}{wC_c(N \cdot U_{in} - V_o)}\right]^2} ; \; t \in [t_4, t_5]. \end{cases} \quad (8)$$

5) Mode 5 $[t_5 - t_6]$: As shown in **Fig. 3(e)**, the primary-side current is the same as that in mode 4 from time t_5. On the secondary side of the transformer, the discharging of buffer capacitor C_c is completed until time t_6, at which time the mode ends. The current through the filtering inductor at time t_3 is $I_{L\max}$, and the duration of mode 4 and mode 5 is

$$\Delta t_{3-6} = \frac{N I_{L\max} L_k}{2U_{in}}. \quad (9)$$

6) Mode 6 $[t_6 - t_7]$: As shown in **Fig. 3(f)**, from time t_6, the currents through two windings i_{p1} and i_{p2} are equal. The clamping capacitor is charged during the freewheeling period. The circulating current is almost invariant because the input voltage and clamping capacitor voltage are equal. The two windings are in series with the clamping capacitor. On the secondary side, all of the rectifying diodes are on, and each diode conducts half of the load current. In the CDD absorbing circuit, the voltage across C_c and D_{c2} is 0, while the voltage across D_{c1} is V_o.

The time duration of mode 6 is

$$\Delta t_{6-7} = \frac{1}{2}(1 - 2D)T_s - \Delta t_{3-6}. \quad (10)$$

From time t_7, S_2 is turned on. In the next half cycle, the operation modes are similar to that of the previous half cycle. For conciseness, we do not include a detailed description of the operation modes.

2.3. Design Considerations

2.3.1. Clamping Capacitor

Compared with the conventional push-pull converter, the use of a clamping capacitor has many advantages for the proposed topology including: 1) the clamping capacitor provides a loop that releases energy when both switches are turned off. This means that it not only clamps the drain-source voltage of switch to two times the input voltage, but it also reduces the loss of the converter and improves the efficiency. 2) The flux imbalance is inhibited. The clamping capacitor performs a charge and discharge process in a cycle, and its voltage is around U_{in}. Assuming that the duty cycle of the switch S_1 increases suddenly, the voltage-second product of the winding N_{p1}

would also increase, which lead to the increment ΔI_m of the exciting current L_m corresponding to the instantaneous current increment ΔI_m through S_1. After S_1 shuts off, the clamping capacitor voltage would increase by ΔU_{in} because of the additional loop current. After S_1 switches on, the voltage across winding N_{p1} will add ΔU_{in} based on U_{in}, which leads to an increase ΔI_m in the demagnetizing current. This can ensure the voltage-second product balance of the transformer in the switching cycle, limiting the flux imbalance.

The larger C_s is, the smaller the voltage ripple will be. When C_s exceeds a certain value, the voltage ripple will be very small; a large capacitance will result in the large size and bad suppression ability of the flux imbalance. When C_s is small, the voltage ripple is obvious and the switching stress of the switch is increased. Thus, the choice of C_s should fully consider the physical circuit characteristics and simulation results. In addition, to satisfy the capacitance requirement, capacitors are typically connected in parallel.

2.3.2. Transformer Leakage Inductor

From Eq. (2), the larger the transformer leakage inductor, the larger will be Δt_{0-1}, the switch turns from off to on, and the switching current time is larger. The larger the value of Δt_{0-1}, the smaller is the effective duty cycle, which decreases the efficiency of the converter. In practical applications, the leakage inductor should be decreased.

2.3.3. Snubber Capacitor

Based on the analysis of the CDD circuit, the snubber capacitor C_c and the leakage inductor in the secondary side of the transformer absorb the inverse peak current of the diode, and the resonant frequency is $w = 1/\sqrt{L_\sigma \cdot C_c}$. If the snubber capacitor is too small, the resonant cycle is too large. The reverse recovery process of the diode has not finished, but the voltage across C_c has reached saturation, which means that the peak absorbing effect is not obvious. If the snubber capacitor is too large, although the peak absorbing effect is good, the discharge time of the snubber capacitor is too large, which affects the PPF converter. In practical applications, the resonant cycle is typically chosen as 1/10 to 1/5 of the switch flux time, and is given as follows.

$$\frac{DT_s}{10} \le 2\pi\sqrt{L_\sigma C_c} \le \frac{DT_s}{5}. \quad (11)$$

3. Controller Design and Performance Analysis

3.1. Development of Mathematical Model

From the analysis in Section 2, we know that the switching cycle of the PPF converter can be classified into 12 modes. For simplification of the mathematical model, we omit the switching process and assume that all switching is finished instantly. There are two modes: 1) switches S_1 and S_2 are on. The equivalent circuit is shown in **Fig. 4**, where two single-side push-pull forward circuits are in parallel; 2) switches S_1 and S_2 are off, where the converter is in circulating-current mode and does not supply energy to the secondary side, which is in follow-current mode. The equivalent circuit is shown in **Fig. 5**.

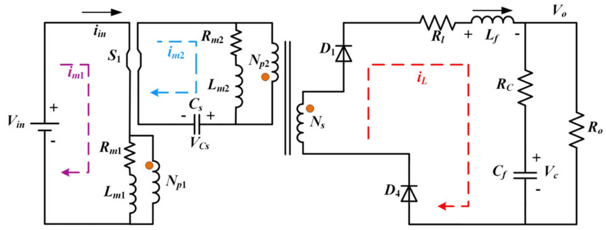

Fig. 4. The switching-on equivalent circuit of the forward push-pull converter.

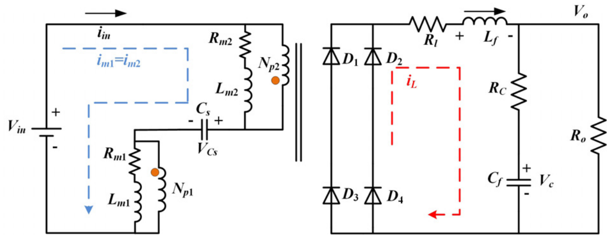

Fig. 5. The switching-off equivalent circuit of the forward push-pull converter.

As the state variable, we choose exciting currents i_{m1}, i_{m2}, clamping capacitor voltage V_{cs}, inductor current i_l, and capacitor voltage V_c, while the input voltage V_{in} is the input variable, and the output voltage V_o is the output variable. The state-space equation of the system is established as follows.

3.1.1. State 1 (Switch S_1 or S_2 is On)

$$\begin{cases} V_{in} = i_{m1}R_{m1} + \dot{i}_{m1}L_{m1} \\ -V_{C_s} = i_{m2}R_{m2} + \dot{i}_{m2}L_{m2} \\ C_s\dot{V}_{C_s} = i_{m2} \\ N \cdot V_{in} = R_l i_l + L_f \dot{i}_l + V_c + R_c C_f \dot{V}_c \\ i_l = C_f\dot{V}_c + R_c C_f \dot{V}_c + \dfrac{V_c}{R_o} \end{cases} \quad (12)$$

The equation can be written as Eq. (13).

$$\begin{cases} \dot{x}(t) = \mathrm{A}_1 x(t) + \mathrm{B}_1 u(t) \\ y(t) = \mathrm{C}_1 x(t) \end{cases} \quad (13)$$

$$x(t) = [i_{m1} \quad i_{m2} \quad V_{C_s} \quad i_l \quad V_c]^T$$
$$u(t) = U_{in}$$

$$\mathrm{A}_1 = \begin{bmatrix} -\frac{R_{m1}}{L_{m1}} & 0 & 0 & 0 & 0 \\ 0 & -\frac{R_{m2}}{L_{m2}} & -\frac{1}{L_{m2}} & 0 & 0 \\ 0 & \frac{1}{C_s} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\left(\frac{R_L}{L_f}+\frac{R_0R_C}{L_f(R_0+R_C)}\right) & -\frac{R_0}{L_f(R_0+R_C)} \\ 0 & 0 & 0 & \frac{R_0}{C_f(R_0+R_C)} & -\frac{1}{C_f(R_0+R_C)} \end{bmatrix}$$

$$\mathrm{B}_1 = \begin{bmatrix} \frac{1}{L_{m1}} & 0 & 0 & \frac{N}{L_f} & 0 \end{bmatrix}$$

$$\mathrm{C}_1 = \begin{bmatrix} 0 & 0 & 0 & \frac{R_oR_c}{R_o+R_c} & \frac{R_o}{R_o+R_c} \end{bmatrix}$$

3.1.2. State 2 (Switches S_1 and S_2 are Off)

$$\begin{cases} V_{in} &= i_{m1}R_{m1} + \dot{i}_{m1}L_{m1} + V_{C_s} + i_{m1}R_{m2} + \dot{i}_{m1}L_{m2} \\ V_{in} &= i_{m2}R_{m1} + \dot{i}_{m2}L_{m1} + V_{C_s} + i_{m2}R_{m2} + \dot{i}_{m2}L_{m2} \\ C_s\dot{V}_{C_s} &= i_{m2} \\ 0 &= R_l i_l + L_f\dot{i}_l + V_c + R_cC_f\dot{V}_c \\ i_l &= C_f\dot{V}_c + R_cC_f\dot{V}_c + \frac{V_c}{R_o} \end{cases} \quad \ldots\ldots\ldots\ldots \quad (14)$$

The equation can be written as Eq. (15).

$$\begin{cases} \dot{x}(t) = A_0x(t) + B_0u(t) \\ y(t) = C_0x(t) \end{cases} \quad \ldots\ldots\ldots \quad (15)$$

where

$$x(t) = [i_{m1} \quad i_{m2} \quad V_{C_s} \quad i_l \quad V_c]^T$$
$$u(t) = U_{in}$$

$$\mathrm{A}_0 = \begin{bmatrix} \frac{R_{m1}+R_{m2}}{L_{m1}+L_{m2}} & 0 & \frac{1}{L_{m1}+L_{m2}} & 0 & 0 \\ 0 & \frac{R_{m1}+R_{m2}}{L_{m1}+L_{m2}} & \frac{1}{L_{m1}+L_{m2}} & 0 & 0 \\ 0 & \frac{1}{C_s} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\left(\frac{R_L}{L_f}+\frac{R_0R_C}{L_f(R_0+R_C)}\right) & -\frac{R_0}{L_f(R_0+R_C)} \\ 0 & 0 & 0 & \frac{R_0}{C_f(R_0+R_C)} & -\frac{1}{C_f(R_0+R_C)} \end{bmatrix}$$

$$\mathrm{B}_0 = \begin{bmatrix} \frac{1}{L_{m1}+L_{m2}} & \frac{1}{L_{m1}+L_{m2}} & 0 & 0 & 0 \end{bmatrix}$$

$$\mathrm{C}_0 = \begin{bmatrix} 0 & 0 & 0 & \frac{R_oR_c}{R_o+R_c} & \frac{R_o}{R_o+R_c} \end{bmatrix}$$

Based on the state-space Eqs. (13) and (15), with the help of the state-averaging method and disturbance method, the small-signal model of the output voltage-to-duty ratio is

$$\frac{\hat{y}(s)}{\hat{d}(s)} = \mathrm{C}(s\mathrm{I}-\mathrm{A})^{-1}[(\mathrm{A}_1-\mathrm{A}_0)x + (\mathrm{B}_1-\mathrm{B}_0)V_{in}] + (\mathrm{C}_1-\mathrm{C}_0)x. \quad \ldots\ldots\ldots\ldots \quad (16)$$

Then, the transfer function of the input voltage-to-duty ratio is

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{NV_{in}R_o}{R_L+R_o} \cdot \frac{(R_cC_fs+1)\omega_n{}^2}{s^2+2\xi\omega_ns+\omega_n{}^2}, \quad (17)$$

where

$$\xi = \left[\frac{L_f+R_lR_oC_f}{(R_l+R_o)} + R_cC_f\right] \cdot \frac{\omega_n}{2}$$
$$\omega_n = \sqrt{\frac{R_l+R_o}{L_fC_f(R_c+R_o)}}$$

Similarly, the transfer function of the inductor current-to-duty ratio is

$$G_{id}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{NV_{in}}{R_L+R_o} \cdot \frac{(R_c+R_o)C_fs+1}{as^2+bs+1}. \quad (18)$$

where

$$a = \frac{L_fC_f(R_o+R_c)}{R_o+R_l}$$
$$b = \left(\frac{L_f+R_lC_fR_o}{R_o+R_l} + R_cC_f\right).$$

3.2. Feedback-Loop Compensation of Push-Pull Forward Converter

As shown in **Fig. 6**, the change in the input voltage or load will cause a small slow change in the output voltage V_o, which will be applied across the negative input side V_f of the error amplifier. It will be compared with the given voltage of the positive side of the converter, and then the output side V_e of the error amplifier will change and be injected into the pulse-width modulated (PWM) regulator and produce PWM signals. Then, through the frequency divider, control signals with a phase difference of 180° will control S_1 and S_2, and form a negative feedback-voltage stabilization system.

In the design of the switching power source, the following requirements should be satisfied: 1) in the frequency across the point, the open-loop phase shift should be less than 360°, and the phase margin should be larger than 45°. 2) In order to prevent the rapid change of the gain-slope

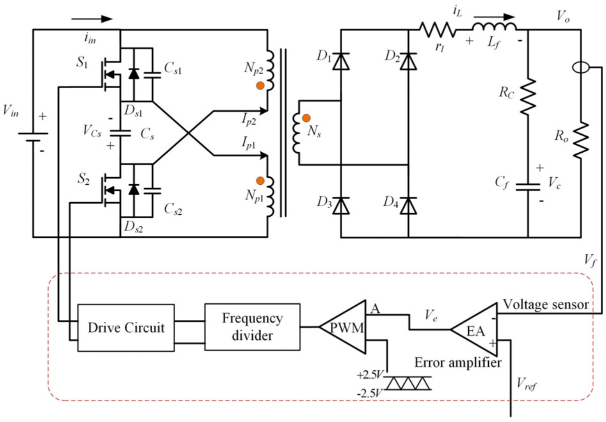

Fig. 6. The closed-loop feedback loop of PPF converter.

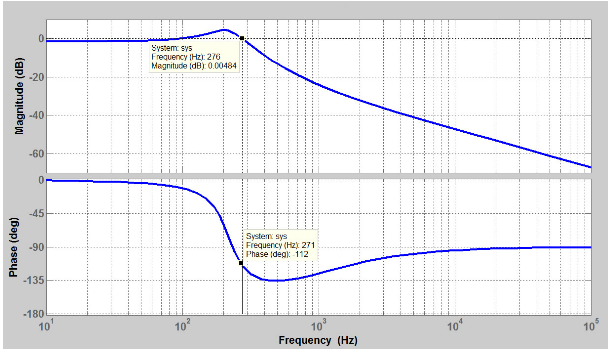

Fig. 7. The system bode plot without loop compensation.

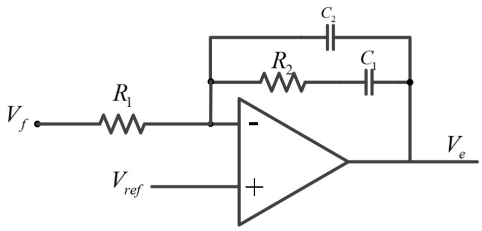

Fig. 8. The feedback network of the quadratic-error amplifier.

circuit, the slope of the open-loop gain at the cross frequency is -1. 3) In the process of switching the power source, in order to prevent large ripples, the cross frequency is defined as 1/4 to 1/5 of the switching frequency.

3.2.1. Frequency Response Without Loop Compensation

a. Sampling Network Gain In the system, the gain of the negative input side of the error amplifier V_r and output voltage is

$$G_{fb}(s) = \frac{V_f}{V_{out}} = \frac{2.5}{30000} \times 200 \times \frac{1.37}{2} = 0.0114. \quad (19)$$

b. Pulse Width Modulator Gain The pulse-width modulator gain is a voltage gain, which compares the DC voltage V_e with a 5 V triangle wave, and then produces a 180° pulse using a frequency divider. When V_e is equal to the smallest voltage of the triangular wave, the duty ratio is zero; when V_e is equal to the peak voltage of the triangular waves, the duty ratio is 50%. Then, the pulse-width gain is

$$G_{pwm}(s) = \frac{\Delta d}{\Delta V_e} = \frac{1}{5}. \quad (20)$$

From the analysis above, by combining Eqs. (17), (19), and (20), the open-transfer function of the output voltage to the duty ratio is :

$$G(s) = G_{vd}(s) \cdot G_{fb}(s) \cdot G_{pwm}(s). \quad (21)$$

The element parameters of the system are chosen as $V_{in} = 100$ V, turn ratio $N = 17/5$, output resistor R_o =25 Ω, output inductor L_f =400 μH, equivalent internal resistor $r_l = 0.15$ Ω, output capacitor C_f =1320 μF, equivalent resistor R_c=0.13 Ω. From Eq. (21), we can obtain the bode plot as shown in **Fig. 7**. We observe that at low frequency, the gain is small, which will result in large steady-state errors. The cut-off frequency is 276 Hz, the middle frequency band is not smooth, and the system dynamic response is not ideal. In practical systems, the switching frequency of the DC-DC converter is 50 kHz. We are typically required to design a loop compensation to ensure that the cutoff frequency is about 10 kHz, and the system has a good steady-state and dynamic response.

3.2.2. Loop-Compensation Parameter Design

The frequency of the system is 50 kHz, and from the cross frequency, the desired cutoff of the switch is 10 kHz. From **Fig. 7**, the system gain at 10 kHz is less than -40 dB without compensation. At the same time, on the left side of the cross frequency, the open-loop gain should be large enough to ensure that the network ripples at low frequency can decay to a very low level. In addition, the open-loop gain in the high-frequency band should decrease rapidly to suppress the high-frequency noise. We chose a quadratic-error amplifier to compensate the loop. The circuit is shown in **Fig. 8**.

The transfer function of the compensation network is shown as

$$G_{ef}(s) = \frac{\hat{v}_e(s)}{\hat{v}_f(s)} = \frac{\left(R_2 + \frac{1}{sC_1}\right) \cdot \left(\frac{1}{sC_2}\right)}{R_1\left(R_2 + \frac{1}{sC_1} + \frac{1}{sC_2}\right)}, \quad (22)$$

which can be further denoted as

$$G_{ef}(s) = \frac{1 + sR_2C_1}{sR_1(C_1 + C_2)\left(1 + \frac{sR_2C_1C_2}{C_1 + C_2}\right)}. \quad (23)$$

In the practical application, C_2 is typically much smaller than C_1. Therefore the transfer function can be simplified as

$$G_{ef}(s) = \frac{1 + sR_2C_1}{sR_1(C_1 + C_2)(1 + sR_2C_2)}. \quad (24)$$

The curve of the error amplifier is shown in **Fig. 9**. There is an initial pole at F_{po}. From the initial pole fre-

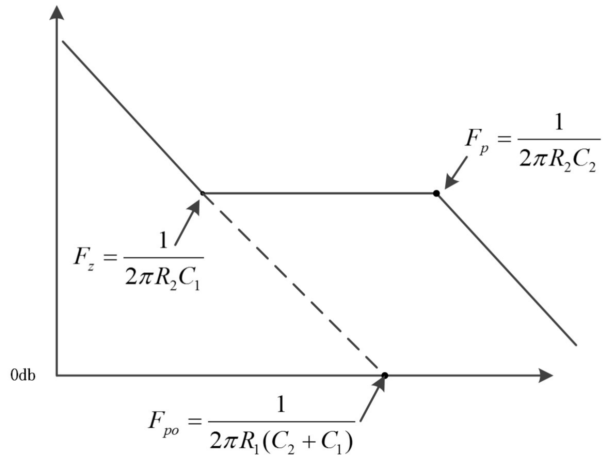

Fig. 9. The gain curve of the quadratic-error amplifier.

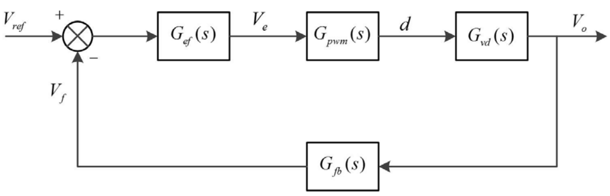

Fig. 10. The closed-loop system control diagram with compensation.

quency 0 db, there is a line with slope -1 to low frequency. Further, there is a zero point that makes the slope from -1 become a horizontal line in order to ensure that the system can be stable at the middle frequency range. At F_z, by adding a pole point, the system can decay rapidly in the high-frequency band. With the design of the compensation network, the control diagram is as shown in **Fig. 10**.

In the compensation-network parameter design, an important issue is to determine the resistor and capacitor values. Based on the cross frequency at 10 kHz, we chose an error amplifier with an amplification of $100x$ to satisfy the $+40$ dB requirement, i.e., $R_2/R_1 = 100$. Based on the Wiener Bohr method, we have $F_{co}/F_z = F_p/F_{co} = K$, where F_{co} is the cross frequency. Then, the expression for C_1 and C_2 can be obtained as

$$\begin{cases} C_1 = \dfrac{K}{2\pi R_2 F_{\text{co}}} \\ C_2 = \dfrac{1}{2K\pi R_2 F_{\text{co}}}. \end{cases} \quad \text{. . . . . (25)}$$

The bode plots of compensation with different K values are shown in **Fig. 11**. We observe that the bode plot has been improved significantly with compensation. The gain is large at low frequencies, remains smooth at middle frequencies, and decreases rapidly at high frequencies. The cross frequency with compensation is between 4–5 kHz, which leaves an adequate phase margin and satisfies the design requirement. Different K values correspond to different adjustment curves. In general, the K value has a small effect on the amplitude frequency. The higher the

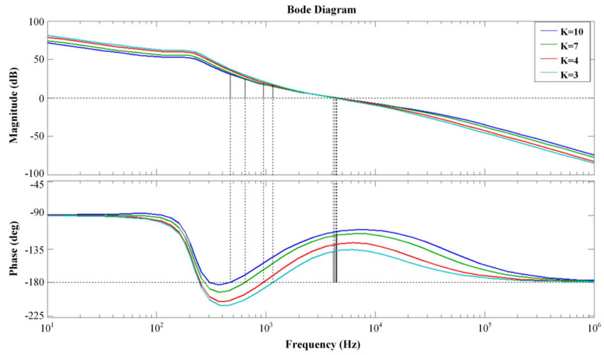

Fig. 11. Bode plots of the compensated system with different K values.

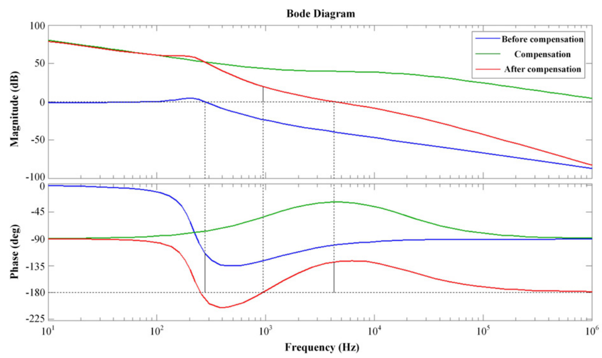

Fig. 12. Comparison of bode plots for compensated and un-compensated systems.

K value, the larger will be the phase margin, but it is not good for the decay of the high-frequency noise. Therefore, when debugging the physical system, the change of resistors and capacitors with the same order of magnitude will not significantly affect the steady-state and dynamic performance. In the designed system, we chose $K = 4$. The compensated bode plot is shown in **Fig. 12**.

3.3. Power-Supply Impedance and Noise Requirements

Because the output of the supply is connected directly to the communication channel, it is important to ensure that the power supply does not degrade the communication performance. In ECP brake systems, the communication frequency ranges from 110 kHz to 138 kHz (C band), and in this frequency band, it is required that the power supply has a high impedance ($\geq 500\Omega$) and low noise on the power line. To meet these requirements, an effective method is a combination of a resonant circuit and LC filter, as shown in **Fig. 13**.

Where R_1, R_2 is the equivalent series resistance (ESR) of the capacitor C_1, C_2, and the resistive damping R is included to degrade the impulse noise from the power line. The inductor L_1, L_2 is important to separate the power supply from the transceiver. The corresponding voltage

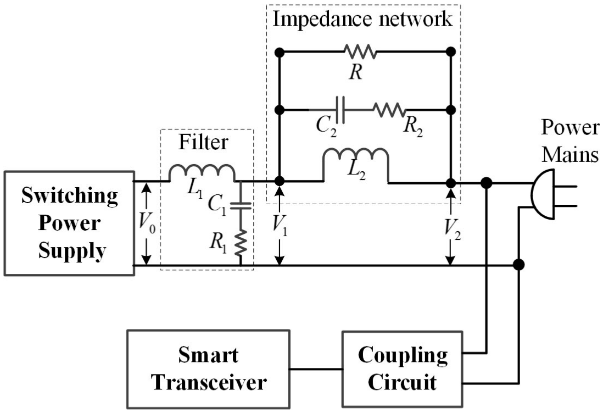

Fig. 13. Reduced attenuation and noise caused by the switching-power supply with a combination of a resonant circuit and LC filter.

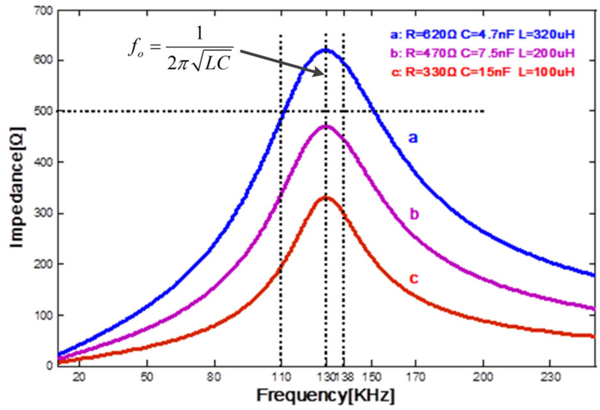

Fig. 15. Impedance of the resonant circuit with different parameters.

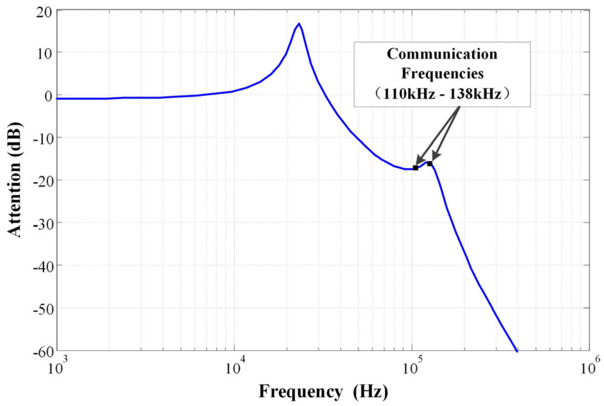

Fig. 14. Output frequency response of the switching power supply.

Table 1. Parameters of the converter.

Parameter symbol	Parameter implication	Value
V_{in}	Input voltage	DC 110 V
$N = N_s/N_p$	Turn ratio of transformer	17/5
V_{out}	Output voltage	DC 230 V
$L_m = L_{m1} = L_{m2}$	Magnetic inductance	290 μH
$L_k = L_{k1} = L_{k2}$	Leakage inductance	1.45 μH
$D = D_1 = D_2$	Duty ratio	0.3
R_L	Output load	23
T	Switching period	20 μs
L_f	Output inductance	350 μH
C_f	Output capacitor	470 μF
C_s	Clamping capacitor	10 μF
C_c	Snubber capacitor	1500 pF

relationship is

$$\frac{V_1}{V_0} = \frac{R_1C_1s+1}{L_1C_1s^2+R_1C_1s+1}$$
$$\frac{V_2}{V_1} = \frac{RR_2C_2L_2s^2+RL_2s}{(R+R_2)C_2L_2s^2+(RR_2C_2+L_2)s+R}. \tag{26}$$

From Eq. (26), we can obtain the output frequency response, as shown in **Fig. 14**. It is obvious that the filter attenuates the switching supply noise in the communication frequency band. In addition, we achieved an output impedance of over 500Ω when we used the parameters $R = 620$ Ω, $C_1 = 4.7$ nF, and $L_1 = 320$ μH, which is shown in **Fig. 15**.

4. Simulation Results

Based on the requirements of ECP power-supply designs, by combining the modeling analysis and principles of the modified push-pull circuit as well as the compensation design for the control loop, we employ professional version of power-electronic simulation software Saber to select the key parameters of the push-pull converter, and to verify its applications as well as advantages.

According to the analysis regarding the modified push-pull converter and the compensation design of the control loop, the relative parameters are shown in **Table 1**. The simulation waveform is as follows.

Figure 16 shows the waveform for the gate-source voltage V_{gs}, the drain-source voltage V_{ds}, as well as two primary-side currents i_{p1}, i_{p2}. The snubber capacitor voltage V_{C_c} and the rectifying diode voltages V_{D1}, V_{D2} on the secondary-side of the transformer are also shown in this figure. We find that the waveforms from times $t_0 - t_7$ are in agreement with the push-pull converter theory waveform in **Fig. 2**. From **Fig. 16**, we can determine that the maximum V_{ds} is two times the input voltage, which illustrates that the clamping capacitance was effective, not only to assimilate the leakage inductance of the primary coil but also decrease to the drain-source voltage of the switch. The theoretical maximum voltage across the snubber capacitors is $V_{C_c} = 2(N \cdot U_{in} - V_o) = 288$ V, which is similar to the waveform obtained in the simulation. The theoretical maximum voltage across the rectifier diode is $V_D = 2N \cdot U_{in} - V_o = 518$ V, which is similar to the waveform in the simulation.

Figure 17 shows the voltage waveforms of lossless

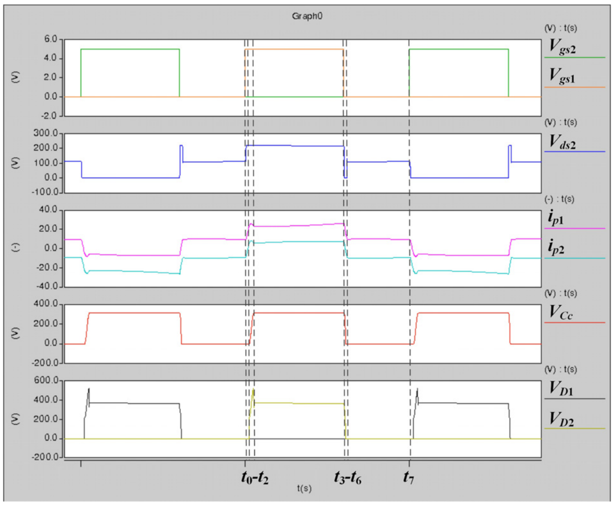

Fig. 16. Simulation result for important waveforms in the modified push-pull converter.

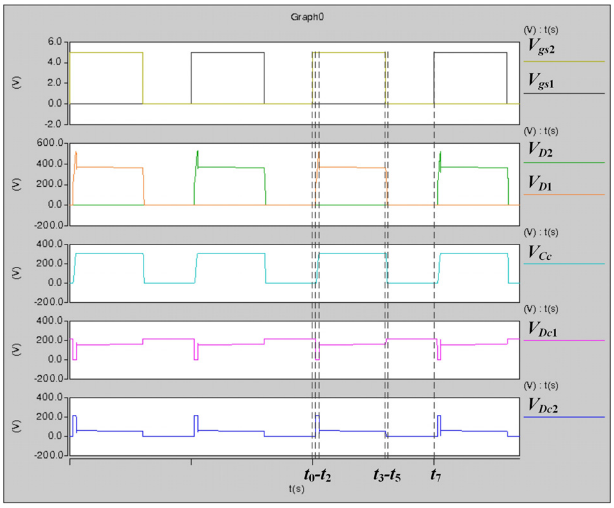

Fig. 17. Voltage-simulation waveforms of lossless absorption CDD in the modified push-pull converter.

absorption CDD on the push-pull converter. The voltage across both capacitor C_c and diode D_{c2} in the post-production phase is zero, and diode D_{c1} sustain the output voltage corresponding to mode1 $[t_0 - t_1]$. Capacitor C_c begins to absorb the reverse peak on the rectifier diode at t_1. At this time, diode D_{c1} conducts, and the voltage on D_{c2} is the output voltage, until the voltage across capacitor C_c becomes a maximum in mode 2 $[t_1 - t_2]$. Starting from t_2, the transformer secondary-side voltage returns to NU_{in} Capacitor C_c has the same voltage, and the respective voltages across D_{c1} and D_{c2} are:

$$\begin{cases} V_{D_{c1}} = N \cdot U_{in} - V_o \\ V_{D_{c2}} = 2V_o - N \cdot U_{in}. \end{cases} \qquad (27)$$

From t_3, the capacitor begins to discharge and the diode D_{c2} switches on, the voltage across D_{c1} is the output voltage until the capacitor discharges completely. Starting from t_5, the CDD circuit stops working, and resumes operation in the second half of the period.

The adoption of a lossless absorption CDD circuit improved the traditional push-pull topology, and aims to decrease the reverse peak voltage of the secondary-side rectifier diode by archiving it in a buffer capacitor. The modified topology can reduce the wastage of the converter as well as improve its output efficiency. The simulation results shown in **Fig. 17** further verified the feasibility of the circuit.

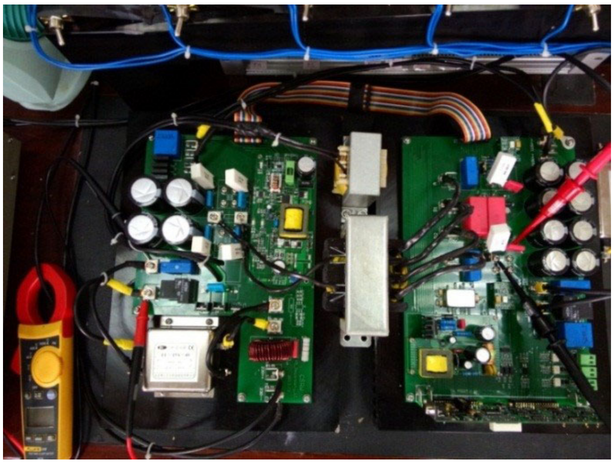

Fig. 18. Image of the experimental circuit.

Table 2. Parameters of the converter.

Circuit parameters	Value
Input voltage	110 V DC
Output voltage	230 V DC
Switching Frequency	50 kHz
Winding ratio	$N_{p1} : N_{p2} : N_s = 5:5:17$
Output power	2300 W
Primary leakage inductor	$L_{k1} = L_{k2} = 1.45\ \mu$H
Output filter inductor	350 μH
Output filter capacitor	560*4 μF
S_1, S_2	IXFN132N50P3
D_1, D_4	DSEP2X31-12A

5. Experimental Verification

In order to verify the control strategy and operation principle of the proposed converter, we built a PPF converter with a full-wave bridge rectifier, as shown in **Fig. 18**. The parameters and specifications are given in **Table 2**.

The experimental waveforms of the proposed converter under conditions of 230 V and 10 A are shown in **Figs. 19** to **21**.

Figure 19 shows the drain-to-source voltage across the switch S_2 and the control signals of the switches u_{s1} (S_1) and u_{s2} (S_2), which go through a drive circuit to generate the gate-signal voltage V_{gs1}, V_{gs2}. We observe that the two switching logic signals operate at 180° out of phase; and the maximum voltage across S_2 is 220 V, which is twice

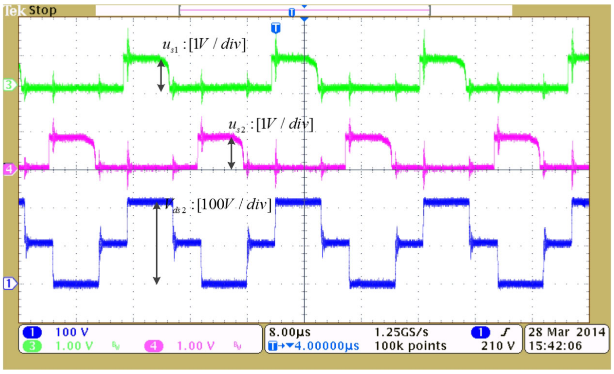

Fig. 19. The drain-to-source voltage across the switch S_2 (V_{ds2}) and the two switching logic signals u_{s1}, u_{s2}.

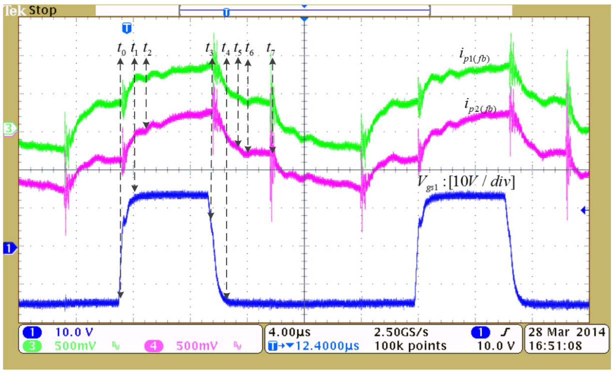

Fig. 20. The gate-to-source voltages $V_{gs1}(S_1)$ and the currents (i_{p1}, i_{p2}) on the primary side of the transformer at full load.

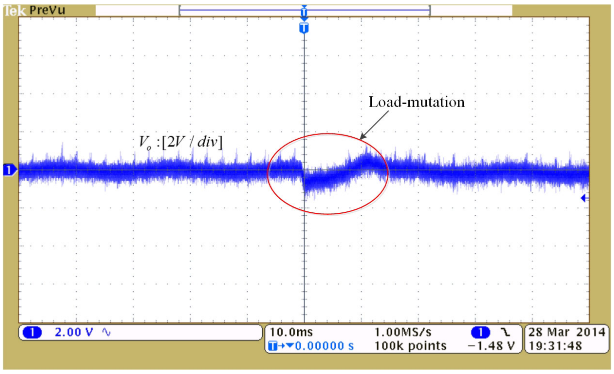

Fig. 21. Transient response to increments in the load (the load increments from 5.45 A to 8.12 A).

that of the input voltage. We can appreciate that the clamp capacitor has a positive impact.

Figure 20 shows the waveforms of the gate to source voltages $V_{gs1}(S_1)$ and the current on primary-side of the transformer, i_{p1} and i_{p2}. The voltage of the gate signal V_{gs1} was -15 V during the dead time of one switch period, because a negative voltage can speed up the switch off process. We observe that the modes about varying currents are the same as the theoretical waveforms in **Fig. 2**; therefore, the experimental results prove the theoretical analysis.

Figure 21 presents the alternating component of the

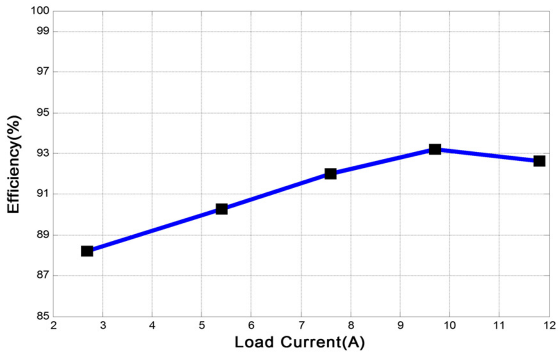

Fig. 22. The efficiency of the proposed converter under different load currents.

output voltage, which recovers rapidly as the load is incremented up from 5.45 A to 8.12 A. This proves that the controller is robust and has good real-time performance.

Figure 22 shows the proposed converter efficiency under a 110 V input voltage with a different load current. It is obvious that the efficiency at the rated operating point (230 V/10 A) reaches 93%. Moreover, the efficiency does not decrease significantly at full load.

6. Conclusion

ECP brake systems have advantages of enabling large freight volumes, short braking times, and good safety for heavy-duty trains. The need for a reliable power supply is essential for the operation of ECP brake systems. In this paper, we proposed an improved PPF converter that has high power, a simple structure, and a high utilization rate of the magnetic core, which is suitable for the application of ECP power supplies. We discussed in detail the operation principles, control method, and performance analysis. In addition, we applied a modified non-dissipative snubber to improve the efficiency and realize a clean power structure. Using the state-space averaging approach, we developed a mathematical model of the converter. We designed a loop-compensation network to verify the steady-state and dynamic performance of the controller. Furthermore, we carefully designed the power supply such that its output impendence does not cause interference with the communication frequency band. The simulation and experiment results demonstrate the effectiveness of the proposed circuit.

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